

REMARKS

These amendments and remarks respond to the Office Action mailed February 14, 2006. Claims 1-3, 6, 8 and 9 have been amended. Claim 13 has been canceled. No new matter has been added. Claims 1-9 are pending in the application. Support for the amendments may be found, by way of example only, in FIG. 2 as well in pages 11-26 of the specification. A petition for a two-month extension of the term for response to said Official Action, to and including July 14, 2006, is transmitted herewith.

In the Office Action, claims 1-6, 8-9, and 13 were rejected as anticipated by Japanese Patent No. 07-141325 to Nakazawa. Claim 7 was rejected as obvious over Nakazawa. These rejections are respectfully traversed.

Nakazawa is directed to a signal processor with a plurality of pairs of register files (11-14) and computing elements (21-24) for parallel processing. Two data selectors 30a, 30b are located between the output of the register files and the input of the computing elements (21-24). Each of the computing elements (21-24) include two input selectors (51a-54a and 51b-54b) coupled between the output of the two data selectors 30a, 30b and the input to each of the computing elements. The data selectors 30a, 30b have one input for each register file and one output to each of the computing elements such that the selectors input data from each of the register files and output to each of the computing elements. In other words, the data selectors 30a, 30b have a single output that is connected to each of the computing elements.

Amended claim 1 recites selecting means having an input from each of the recording means and an output to only one of the operating means, the selecting means inputting the arithmetic elements recorded in each of the recording means to the one operating means. In Nakazawa, the data selectors have an input from each of the register files and an output to each

operating means. Nakazawa fails to disclose or suggest a selector means having an input from each of the recording means and an output to only one of the operating means, the selecting means inputting the arithmetic elements recorded in a selected one of the recording means to the one operating means. Thus, Nakazawa fails to disclose or suggest all of the elements of amended claim 1.

Moreover, Nakazawa fails to disclose or suggest the claimed invention for the following additional reasons. The present invention is directed to a parallel arithmetic apparatus that can perform both matrix operations and inner product operations. In contrast, Nakazawa is configured to execute parallel processing of matrix operations. All of the components in Nakazawa, including data selectors (30a, 30b) and input selectors (51a-54a and 51b-54b), are essential to solve the problem described in Nakazawa: the parallel processing of color conversion and parallel processing of a transposed matrix. Because Nakazawa is designed for one specific purpose that is completely different than the purpose of the claimed invention, one skilled in the art would not be motivated to modify the invention of Nakazawa to arrive at the invention of claim 1. Claims 2-5 depend from claim 1 and should be allowable for at least the same reasons given above for claim 1.

Similarly, amended claim 6 recites a parallel arithmetic apparatus with a plurality of recording means, a plurality of operating means, and selecting means having an input from each of the recording means and an output to the predetermined operating means. For at least the reasons above, Nakazawa fails to disclose or suggest all of the elements of claim 6.

In a similar manner as above, claims 8 and 9 have been amended to recite an entertainment apparatus that performs image processing using a plurality of registers, a plurality of sum-of-products operators, and a single selector having an input

from each of the registers and an output to the predetermined sum-of-products operator. For at least the reasons above, Nakazawa fails to disclose or suggest all of the elements of claims 8 and 9.

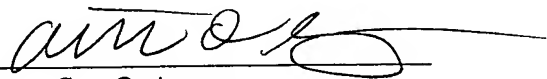
Claim 7 was rejected as obvious over Nakazawa. Claim 7 is asserted as patentable at least for the reasons discussed above in connection with claim 6, upon which claim 7 depends.

As it is believed that all of the rejections set forth in the Official Action have been fully met, favorable reconsideration and allowance are earnestly solicited. If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he/she telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he/she might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

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